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Statistical analysis using AI-ML enabled SPICE solution to get tail samples for high linearity delta sigma converters

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Motivation

- Continuous Time Delta-Sigma Modulators must achieve high linearity while maintaining efficiency in area usage and power consumption.
- In Sigma-Delta Converters, multi-bit quantization is preferred in high resolution designs to limit the clock frequency and hence the associated power.
- Multi-bit quantization comes with a penalty of linearity due to mismatch between the multiple elements.
- Dynamic Element Matching techniques are used to overcome the challenge of linearity.

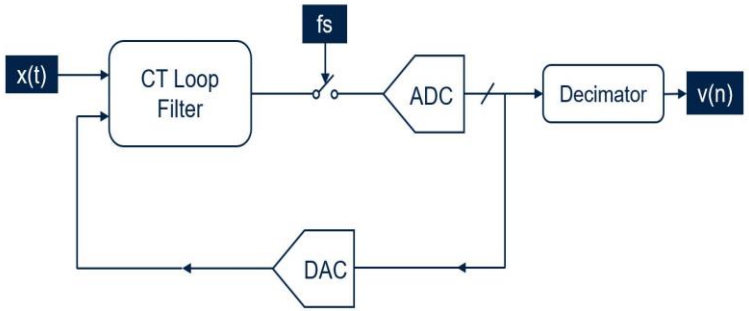

Figure-1 Continuous Time ΔΣ ADC

Motivation

- The mismatch errors between the multi-bit DAC elements limits the linearity, which is inversely dependent on the size of the unit element (e.g. resistor for resistive DACs).
- Statistical analysis is inevitable to determine the linearity for a particular DAC element size to get yield information.
- With stringent area requirements, it is desired to use a minimally sized DAC element and maximize the benefit of DEM technique.

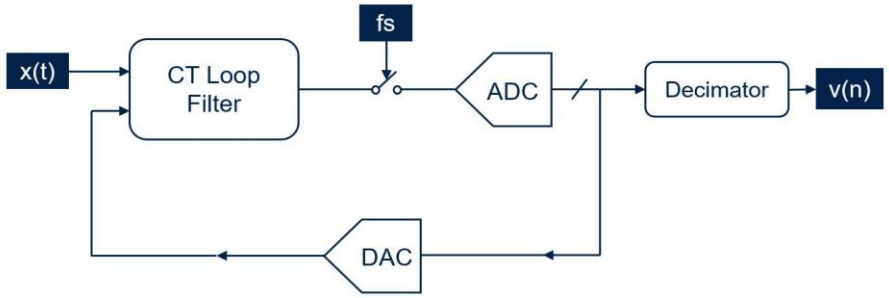

Figure-1 Continuous Time ΔΣ ADC

DEM Technique

- In DEM technique, all the elements are selected in a rotational manner.
- They provide a first order shaping to the spectral tones and thus improve the linearity significantly.

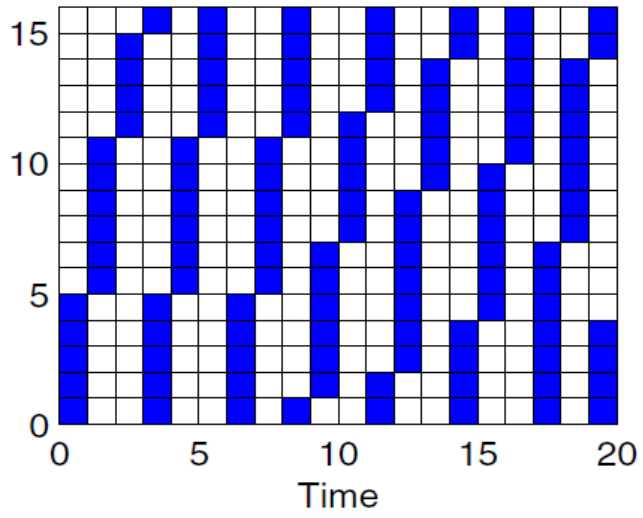

Figure-2 DEM Technique

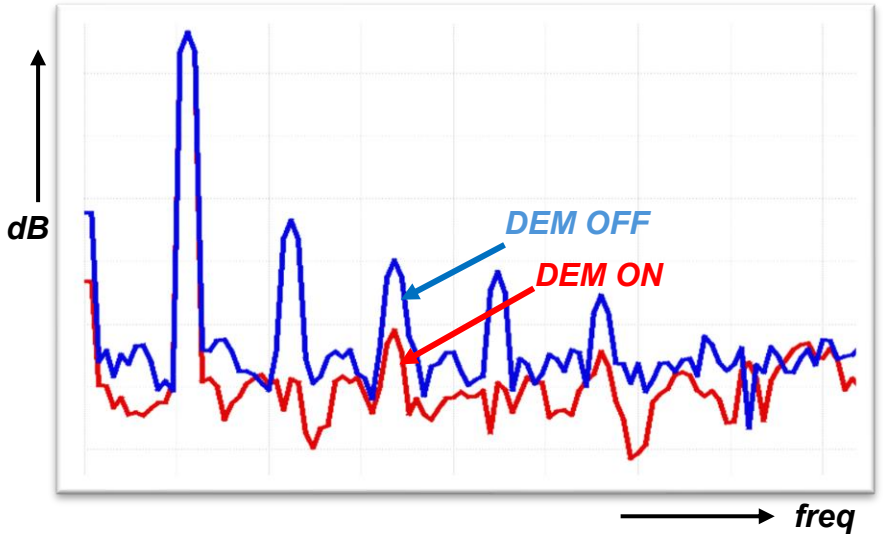

Figure-3 Comparison between DEM ON and OFF

Existing Challenges

Long simulation time leads to high simulation cost and compute resource requirements

Less number of BFMC samples are run by keeping margin in DAC elements area leading to overdesign.

Need for a solution to accurately estimate worst-case Samples with Fewer Simulations

Figure-4 Long tail sample representation in gaussian distribution

Image Source: FMC white paper, Cadence Design Systems

Proposed Solution

Spectre FMC Analysis for worst tail Samples Estimation

- Perform a few random Monte Carlo (MC) simulations to create a mathematical Response Surface Model (RSM) using a machine learning kernel in the Spectre environment.
- Reorder samples from worst to best based on model predictions aligned with measurement goals.
- Simulate the predicted worst iterations to estimate the predictive model error and assess sample reordering quality.
- Update the RSM with this information and predict values for the entire sample space.
- This process identifies the worst samples for measurement-specific goals, providing metrics like sigma, iteration number, and value for effective debugging.

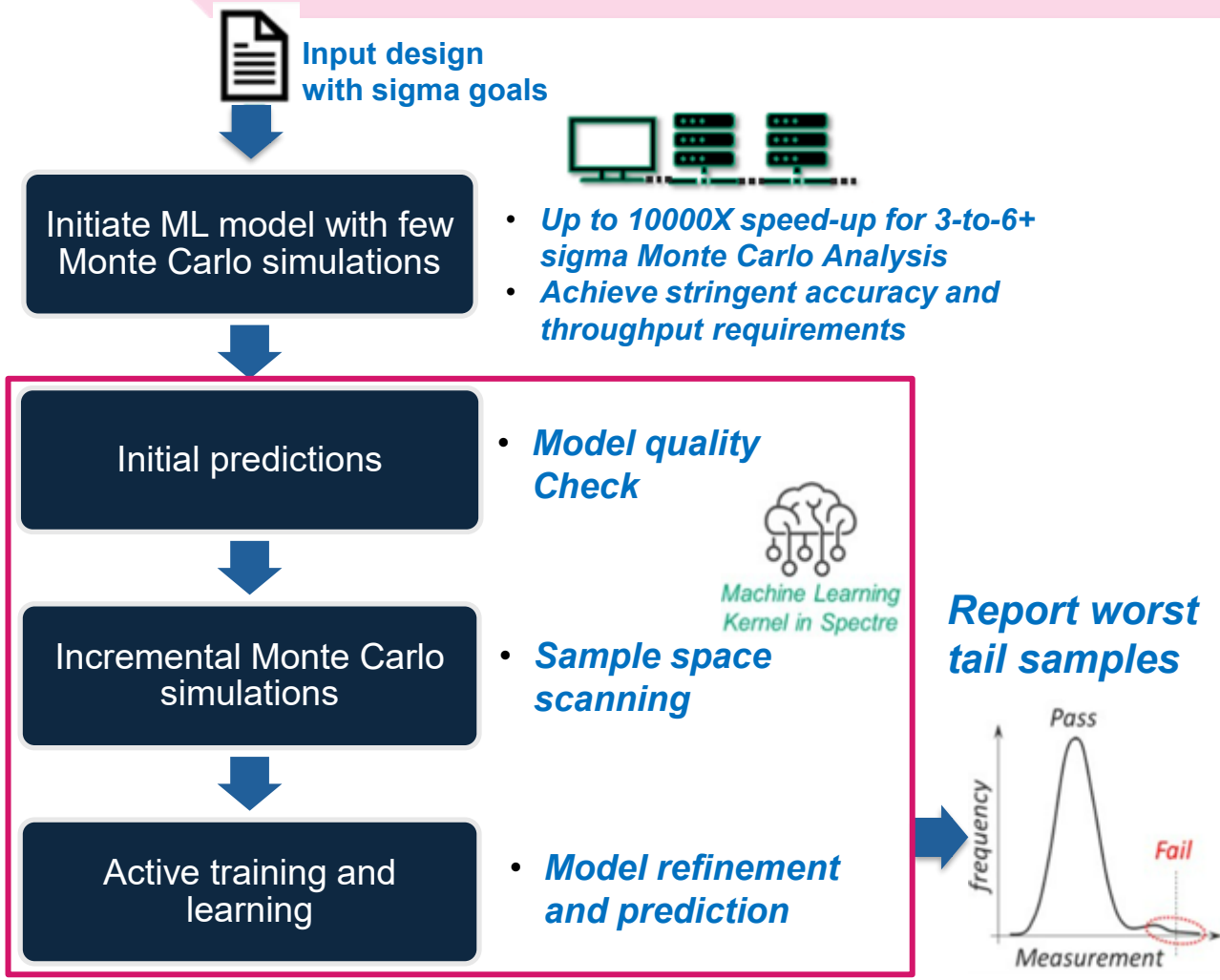

Figure 2: Worst-case sample identification algorithm used in Spectre FMC Analysis

Setup for Spectre-FMC

- Define the goal for FMC analysis: The specs defined in measurement expressions in ADE output setup.
- In the ADE Monte Carlo setup form, select Method as **FMC Worst Samples**.
- After setting up target yield, specify **any one** of the two options below,
  - **Total Samples** (equivalent netlist option is numruns)
  - **Tail Samples** (equivalent netlist option is fmcnumtailsamples).
- The other option will be auto-filled by tool based on table below,

Total Samples	Target Yield	Tail Samples (reported by FMC)	Sigma Range
20K	3	28	(2.99, 4.06)
100K	4	4	(3.98, 4.42)
1M	4.2	14	(4.2, 4.89)
100M	5.4	4	(5.39, 5.73)
500M	5.8	3	(5.73, 6)
1B	5.8	4	(5.79, 6.11)

Table 1:relation between the fields, Max Points, Target Yield, and Tail Samples for FMC method.

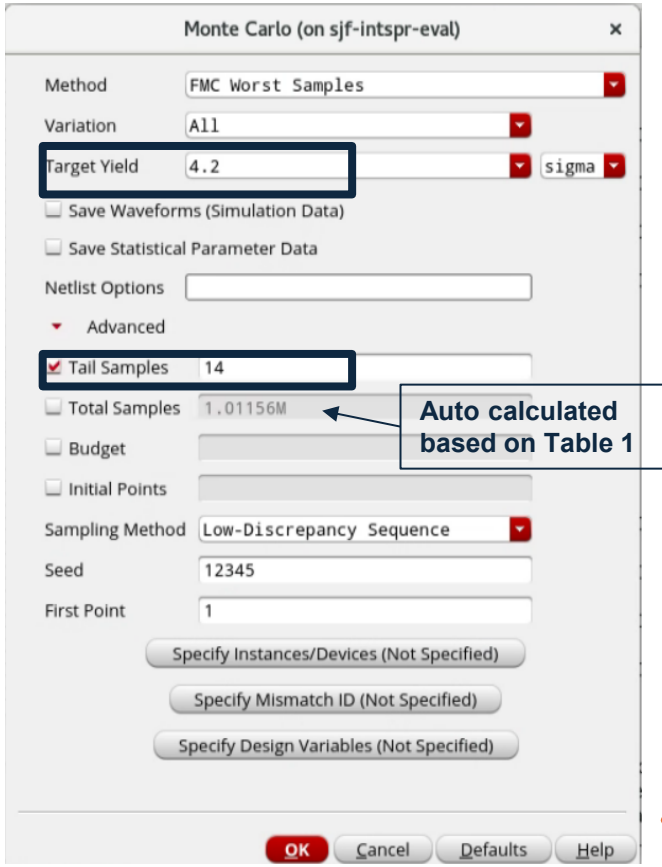

Figure 3: FMC setup form in Virtuoso-ADE

Results

Target SFDR value=90dB	3 sigma			
	BFMC	BFMC (existing flow)	FMC (proposed flow)	
No. of samples required	10K	10K	10k	
Actual simulated runs	10k	500	1100	1050
DAC element Area	A	A	A	A/4
Measurement of SFDR	-	97	94	92
Run Time (10 jobs in parallel)	63 days (not feasible to simulate)	3 days	5.8 days	5.6 days

- To get the actual exact tail sample for worst case SFDR, it is nearly impossible to run BFMC due to its high cost and compute resource requirements.
- As a tradeoff, BFMC is run only for a few samples and margin is kept for the actual worst SFDR value which leads to overdesign.
- With FMC, with only fewer samples, we were able to achieve exact tail sample for 3sigma accuracy.
- The above capability of FMC enables the designer to reduce the area of DAC element (A/4 in this case) confidently while achieving 3sigma yield to meet the target SFDR value.

Conclusion

- The current methodology lacks adequate assurance for designers, prompting excessive overdesign to achieve target specifications dictated by statistical analysis, such as SFDR.

- The proposed Spectre-FMC flow efficiently captures extreme tail samples for 3-sigma accuracy with fewer samples, empowering designers to refine the design and reduce IP area.

4X reduction in DAC element area

9X reduction in number of samples

Multifold saving in compute resources

Seamless integration in Virtuoso-ADE flow

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